

DESTINATION DIRECTED PACKET SWITCH ARCHITECTURE FOR A 30/20 GHz FDMA/TDM GEOSTATIONARY COMMUNICATION SATELLITE NETWORK

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Abstract

This paper concentrates on a destination directed packet switching architecture for a 30/20 GHz FDMA/TDM geostationary satellite communications network. Critical subsystems and problem areas are identified and addressed.

Efforts have concentrated heavily on the space segment; however, the ground segment has been considered concurrently to ensure cost efficiency and realistic operational constraints.

Introduction

In the mid 1980's NASA began the Advanced Communication Technology Satellite (ACTS) program to develop a 30/20 GHz geostationary communication satellite to be launched in 1993. This satellite will open up the Ka-band frequency for commercial communications, develop multibeam and hopping-beam antennas, and demonstrate onboard processing technology. The ACTS system utilizes time division multiple access (TDMA) uplinks and time division multiplexed (TDM) downlinks. One of the drawback of TDMA uplinks are that the ground terminals are forced to transmit at a much higher data rate than there actual throughput rate. For example, in the ACTS system, a ground terminal wishing to transmit a single voice channel at 64 kbps would have to transmit at a burst rate of 27.5, 110, or 220 Mbps (ref. 1). This, in effect, drives the cost of the ground terminals up dramatically by requiring either substantially higher power transmitters or larger antennas, both which are major cost

drivers in a low cost ground terminal. Realizing this, recent emphasis has been place on driving the cost of the ground terminals down. One way to accomplish this is to eliminate the need for high power transmitters on the ground by allowing the user to transmit at a lower data rate using a frequency division multiple access (FDMA) uplink architecture. TDM is chosen for the downlink transmission technique because the high power amplifier (HPA) can be operated at maximum power thereby increasing the downlink signal strength which, in turn, enables the use of very small aperture terminals or VSATs (ref. 2).

Currently, NASA envisions the need for meshed VSAT satellite communications systems for direct distribution of data to experimenters and direct control of space experiments. In the commercial arena, NASA envisions a need for low data rate, direct to the user communications services for data, voice, FAX, and video conferencing. Such a system would enhance current communications services and enable new services. For this type of satellite systems to exist, it must be cost competitive with terrestrial systems at the user level while enhancing the existing quality of service. The key to making this system cost competitive is to drive the cost of the ground terminals down and spread the cost of the satellite among tens or thousands of users. NASA has completed and is continuing to performed a number of studies on such communication systems (ref. 3-6).

Meshed VSAT satellite networks can be

implemented using either a circuit switched architecture, a packet switched architecture, or a combination of the two. Intuitively, it appears that a circuit switched network would be far simpler to implement; however, a packet switch has many potential advantages relative to circuit switching. Therefore, the Digital System Technology Branch at NASA LeRC is currently investigating a packet switched satellite network in order to identify the common subsystems of a circuit and packet switched network and to quantify the complexity of a packet switched network versus a circuit switch. This paper is a direct result of those studies.

The paper will describe the overall network requirements, the network architecture, the protocols and congestion control, and the individual subsystems of a destination directed packet switched geostationary satellite network for commercial communications.

Network Requirements

In order to begin designing the conceptual satellite architecture a list of salient requirements has to be created. The requirements follow: First, the system has to be economically viable and cost competitive with existing terrestrial telecommunication systems while enhancing existing services and adding new ones. Second, the system must provide voice, data, FAX, datagram, teleconferencing, and video communications services. In order to provide these services, the ground terminals will either transmit fixed length packets at 64 kbps or transmit continuously at 2.048 Mbps. It is envisioned that at 2.048 Mbps, the required service will be trunked continuous transmission circuits analogous to the present practice of leasing dedicated T1 circuits. Third, the system will be capable of

point-to-point, multicast, and broadcast transmission. Multicast capability is a necessity in order to provide teleconferencing and video conferencing services. Broadcast transmission may not be necessary but is desirable. The requirement to communicate to every user in the system simultaneously (broadcast) verses only a select number of users within the system (multicast) is not readily apparent. Fourth, the satellite has to accommodate destination directed packets on a packet-by-packet basis. There does not appear to be any advantage to using packets versus a simple circuit switch through a satellite system unless they are destination directed -- the packet destination is contained in each header. For example, the use of packets to set up a virtual circuit simply adds the complexity of packet synchronization and processing to what is actually a circuit switch. Fifth, the satellite will not drop packets. Due to the long round-trip delay times to geostationary satellites, 250 msec, if packets are dropped, the window for requesting a retransmission and the data buffering involved becomes quite undesirable.

Network Architecture Description

The network consists of meshed VSATs operating at 30/20 GHz, transmitting through a processing satellite. Transmission is FDMA up and TDM down. There are eight uplink beams and eight downlink hopping beams covering CONUS. Each downlink beam has eight dwell locations. Associated with each uplink beam is a multi-channel demultiplexer/demodulator capable of demultiplexing and demodulating one thousand and twenty-four 64 kbps channels, a packet synchronizer, a decoder, and a MCDD-to-switch formatting buffer. Associated with each downlink is a switch-to-TDMA formatting buffer, an encoder, and a 150 Mbps burst modulator. The NxN

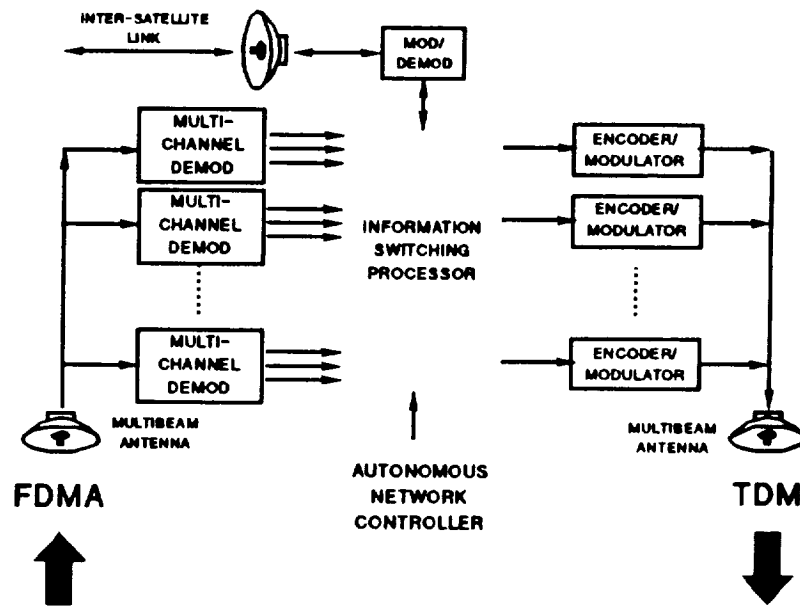


Figure 1 FDMA/TDM Network

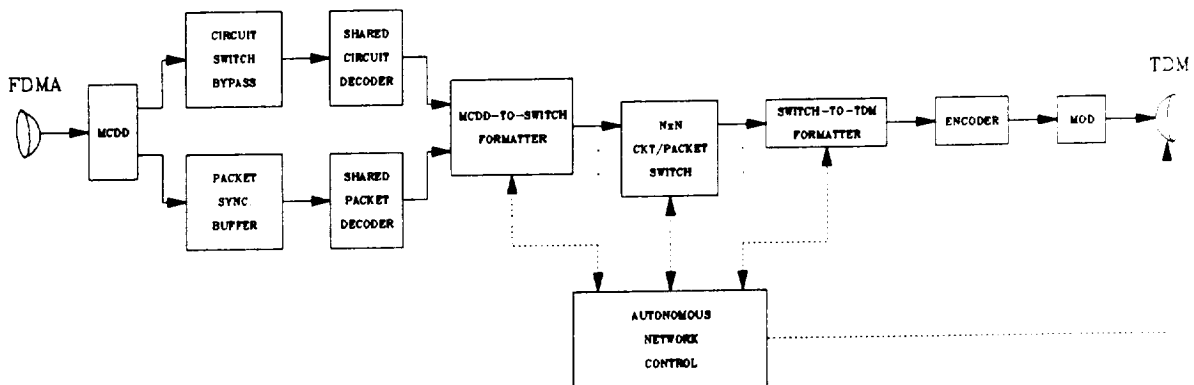


Figure 2 ISP Detailed Architecture

switch performs the spacial switching functions while the formatting buffers perform the temporal switching. The switching, routing, and congestion control are the responsibility of the autonomous network controller onboard the satellite. (fig. 1 and 2)

Many of the relative numbers used to establish the network size and data rates are taken from an architecture study perform by TRW. This report includes a complete link budget and hardware analysis in sufficient detail to estimate size, weight, and power requirements for the satellite and ground terminals (ref. 7).

Protocols

Initial Access

Initial access into the system would be via a reserved signalling channel. One channel for each multichannel demultiplexer would be reserved for requesting entry into the system. This channel would be set up in a slotted aloha format (ref. 8) and accept 64 kbps packets containing a request for a data transmission rate corresponding to either 64 kbps packet data transmission or 2.048 Mbps circuit transmission. Additional information that may be conveyed during initial access would be related to type of data being transmitted (voice, video, FAX, datagram, etc...) and the effective data throughput rate. This information may be useful to the autonomous network controller in order to anticipate and correct for congestion problems. Also, during initial access, the ground terminal will have to specifically request for multicast or broadcast services. This is necessary in order to verify that the downlink capacity can handle the request and to properly bill the user for these services. For broadcasts and multicasts, the

satellite will have to be capable of duplicating the received message up to 64 times onboard the satellite and place that information in to correct downlink beam and dwell.

Upon reception of the initial access request, the satellite will respond via a downlink inband orderwire message as to request granted or denied and a corresponding frequency allocation.

Packet Formats

For 64 kbps packet transmission, the ground terminal will translate incoming data -- be it packets, voice, continuous data, etcetera -- into packets that are specific to the satellite network. The data packets are fixed length in order to simplify the onboard processing. All flow control, acknowledges, and buffering are performed at the ground terminal. There are six fields specific to the packet: synchronization, destination address, source address, control, information, and parity (fig 3).

The synchronization field is used to determine the start of the packet. This field is only necessary in an asynchronous packet network where no timing structure is overlaid on the transmitting portion of the ground terminals. The synchronization field has to be long enough to reduce the probability of a false detection without being so long as to dramatically increase the packet overhead. Presently, this field is 32 bits long.

The destination address field specifies the downlink destination which consists of the downlink beam and the dwell location within that beam. Twenty-six bits are reserved for this corresponding to the eight downlink beams, eight dwell locations within each beam, and 1024 possible ground terminals.

SYNC HEADER	DESTINATION ADDRESS	SOURCE ADDRESS	CONTROL	INFORMATION	PARITY
1 32	33 58	59 74	75	76	
32 BITS	26 BITS	16 BITS	1 BIT	TBD BITS	TBD BITS

Figure 3 Packet Format

The source address field specifies the uplink source. Sixteen bits are reserved for this: three specify the uplink beam, ten specify the uplink frequency corresponding to the transmitting ground terminal; and three specify one of eight multiplexer input ports where up to eight active users may share one ground terminal simultaneously.

There is a one bit control field that indicates whether or not the packet contains useful information or is a dummy packet. Dummy packets are not passed on to the switch but are simply used by the demodulator to maintain lock.

The information field contains communications data that is being passed from ground terminal to ground terminal. This can be continuous transmission data such as voice or standard packets that have the satellite network packet structure overlaid. The length of the packet has not been determined at this time. The tradeoff on packet length is between improved packet efficiency and increased onboard storage. The longer the packet the greater the packet efficiency due to a reduction in the overhead-to-information ratio; however, the longer the packet the greater the onboard storage requirements.

The address, control, and information fields are error correction encoded and that information is placed in the parity field. The length of the parity field has yet to be determined

but is directly related to the length of the information field and the bit error rate required for the address field. The BER for the address and control fields should be at least two orders of magnitude better than the overall network BER of 10^{-7} in order to guard against misrouted or dropped packets. Thus, an overall BER performance of approximately 10^{-9} is required for the address and control fields. The information field will receive this link quality by default.

The idea of increasing the data content in the address and control fields and using two for three majority voting to guarantee 10^{-9} BER performance in those fields was contemplated, discarded and replaced with the concept of using added parity. This was done to reduce the complexity of the onboard processing. It is assumed that the information data field will have to be encoded in order to maintain an overall end-to-end BER performance of 10^{-7} regardless of how the address and control fields are treated. Therefore, it appears to be more efficient to combine the address, control, and information fields together before encoding on the ground. Although a formal analysis has not been done, it appears that less parity bits are required to encode all three fields than to triple the address and control fields for use in majority voting and still require parity bits for encoding the information field -- albeit not as heavily as the combined encoding

requires. In addition, by heavily encoding the combining the address, control and information fields, no two-for-three majority voting circuits need be implemented.

TDM Frame Structure

The TDM frame structure has yet to be defined in detail. The TDM frame will be between one and 32 milliseconds in length. The frame efficiency increases with frame length. However, a longer frame requires greater onboard storage capability. Also, the packet length will directly effect the frame length. Since the downlink location capacity is limited by the size of the packet and the dwell time, if the packet size is large, the dwell time and frame length must be large in order to handle a reasonable number of packets per downlink dwell location. In addition, by making the dwell time and frame length as long as possible the hopping beam antenna system will not be required to switch as often, thus, improving system efficiency.

A superframe structure will be place over the TDM frame structure. Various orderwire messages will be reserved for particular frames within a superframe.

Downlink Orderwire Message Format

Orderwires will be used to convey satellite switch status, system timing information, initial access granted and denied messages, etcetera. The downlink orderwire message will be the first message of each dwell.

Contention and Congestion Control

In a destination directed packet satellite network, contention and congestion control are major concerns.

Contention problems appear in the NxN beam-to-beam switch. The beam-to-beam switch along with the MCDD-to-switch buffer must be design so that contention is avoided within this portion of the switching system (i.e. two or more inputs may not attempt to route to the same output at the same time).

Congestion occurs when more information is destined for a specific downlink/dwell than is available. This occurs because the data packets are self-routing and the routing information is not available until the packet arrives at the satellite. Because of the long propagation delay from the satellite to earth (125 msec), handshaking and requests for retransmission are impractical. In addition, since there is limited storage capability on the spacecraft, buffering of numerous packets for thousands of user is also impractical. Therefore, a congestion control method has to be developed that is specific to this destination directed packet switched satellite system.

Presently, two methods have been identified to deal with this problem.

The first method deals with this problem by simply denying access into the network based upon an analysis of the current state of the switching system and a statistical prediction of the additional capacity that would be required by the new user. In this scenario, during initial access, the user would inform the network control as to the destination of the message, the anticipated mean, mode, and peak data throughput requirements, and a request for point-to-point, multicast, or broadcast service. The network control would then take this information and determine whether or not there was enough capacity available to support the request. Using this method, the packets would be destination directed; however,

each packet would have to be sent to the same destination. Anytime the destination changes, a new request for access must be performed. There are two major drawbacks to this congestion control method: it would be extremely computational intensive to keep track of the statistical nature of each user's data, and the method precludes multiplexing users at the ground terminal.

A second method relies on distributive flow control at the ground terminals. In this scenario, the network control will continually monitor the downlink burst buffers to determine the current capacity of each downlink/dwell location. The network control will periodically transmit information regarding the current state of the downlink buffers to the ground terminals. This information will indicate the relative capacity of each downlink/dwell. For instance, downlink beam one dwell location three may be at 70 percent capacity while downlink beam seven dwell location six is at 90 percent capacity. The network control will set a threshold for capacity at perhaps 85 percent. Once that threshold is exceeded, no new transmissions are permitted to that downlink/dwell location. Communications that were already in progress to downlink beam seven, dwell six are allowed to continue; however, no new transmissions may be sent to this location until the capacity falls below 85 percent. Meanwhile, any user may transmit to downlink beam one dwell location three since its capacity is already under the 85 percent threshold. It is up to the ground terminals to institute the flow control. The threshold is set via the network control in order to allow the ground terminals adequate time to institute flow control before there is a congestion problem in the downlink burst buffer. One advantage that

this method has over the previous is that only the downlink burst buffers need to be monitored in order to determine the state of the switch instead of compiling statistics for every user in the system. A second advantage is that this method allows individual packets to be routed to different destinations; thus, enabling multiplexing of users at the ground terminal. One potential disadvantage may be that the threshold would have to be set to such a conservative number that the satellite capacity may be under severely utilized.

Network Hardware

Ground Terminals

The ground terminal is composed of and indoor and outdoor units (fig. 4).

The indoor unit consist of a terrestrial interface, protocol converter, packet assembler, encoder, continuous modulator, burst demodulator, decoder, message assembler, orderwire processor, and timing and control circuitry.

The ground terminals will interface to the terrestrial telecommunications network at the DS0 (64 kbps), ISDN basic service rate, 2B+D (144 kbps), and T1-type rates (1.544 Mbps or 2.048 Mbps). In addition, the ground terminal will be capable of interfacing to commercial communications equipment and will be compatible with commercial standards.

The protocol converter provides an interface between the commercial communication packet switching standards and the internal packet switching protocol. All hand shaking, acknowledges, and flow control with the terrestrial networks will occur here.

The packet formatter breaks (or

appends) commercial packets into packets of constant length. The source and destination address and the control fields are appended to the fixed length packets and this total package is encoded. At this point, the synchronization bits are appended to the front of the packet and the information is passed on to the modulator.

The modulator and demodulator are two completely separate units. Presently, it is envisioned the uplink modulator will produce an offset QPSK signal and transmit continuously at either 64 kbps or 2.048 Mbps. Filtered OQPSK is used on the uplink in order to obtain a bandwidth efficiency of approximately 1.45 to 1.6 bits/sec/Hz. On the downlink, a burst demodulator is required. The modulation format has yet to be determined, but the data

rates will be in the 150 - 180 Mbps range.

The message assembler reads the demodulated data, strips off the source address fields and reassembles the orderwire messages and any messages destined for that ground terminal. The reassembled messages are then passed on to either the order wire processor or the protocol converter for entry into the terrestrial communications network.

Since this communications network utilizes time division multiplexing on the downlink with bursted data transmission in the 150 Mbps region, the timing and control of the communication is critical. The timing and control system (T&CS) is responsible for obtaining and maintaining synchronization with the satellite. The T&CS informs the

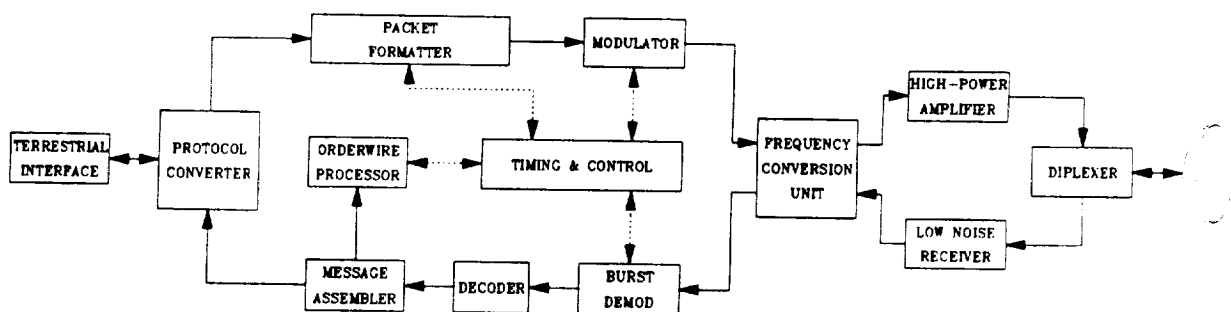


Figure 4 Ground Terminal

burst demodulator of the approximate time of burst arrival and receives a signal indicating actual burst arrival times. The T&CS uses the information obtained from the demodulator to adjust the ground terminals receive side timing in order to synchronize the ground terminal to the network. The T&CS also receives network control information from the orderwire processor and uses this information to determine what type of information is entered into the control fields of the transmitted packets. In addition, the T&CS will turn off the transmitter and modulator during periods where the ground terminal has relinquished access to the satellite uplink channel.

The outdoor unit contains the RF equipment consisting of the frequency conversion system, high power transmitter, diplexer, antenna system, and low noise receiver. The HPA is required to produce approximately 2 watts of transmit power. The required noise figure for the LRN is approximately 2.6 dB. The outdoor unit comprises the majority of the ground terminal cost.

MCDD

On-board demultiplexing and demodulation of narrowband traffic will be provided by multichannel demultiplexer demodulators (MCDD). In general, the MCDD can be viewed as a multifrequency channelizer and a demodulator system. The channelizer operates relatively independent of the modulation scheme; although some optimization for the channelizer may be performed if the modulation format has been identified early on. The demodulator system is either a time shared demodulator, a bank of individual demodulators, or a combination of the two.

The MCDD has been identified as a critical subsystem which needs to be

developed for a FDMA/TDM architecture. Acousto-optical, optical, and digital signal processing technologies have all been identified as candidates for implementing a MCDD. NASA is investigating each of these approaches through contacts, grants, and in-house activity.

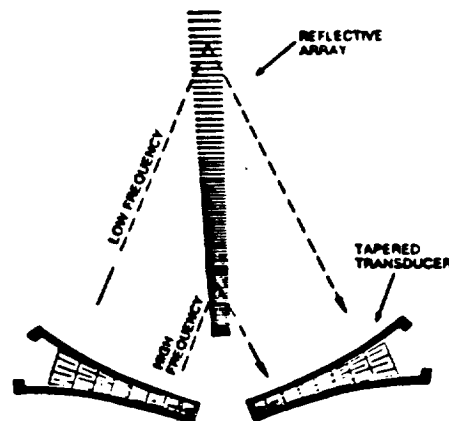


Figure 5 Hyperbolic Reflective Array Compressor

Amerasia Technology Incorporated is in the second phase of a Small Business Innovative Research Contract, NAS3-25862, to developing a proof-of-concept (POC) multichannel demultiplexer (MCD). The MCD uses a convolve-multiply-convolve technique to perform the demultiplexing function and is implemented using a surface acoustic wave herring-bone shaped reflective array compressor with hyperbolically shaped transducers (fig. 5).

Westinghouse Electric Corporation Communications Division is under contract to NASA LeRC (NAS3-25865) to develop a POC MCD which demonstrates the capability of demultiplexing 1000 low data rate FDMA uplinks. The multichannel demultiplexer is implemented as an coherent acousto-optic RF spectrum analyzer utilizing

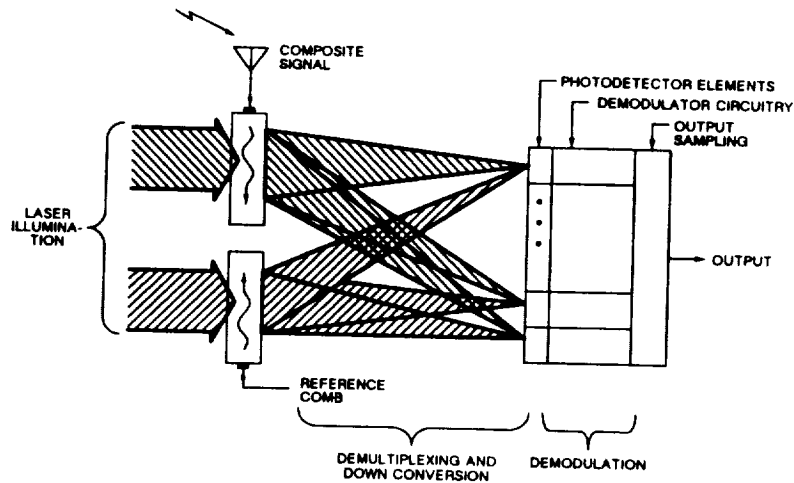


Figure 6 Optical MCDD

heterodyne detection with a modulated reference (fig 6). Similar to the RAC SAW implementation, the optical MCD is expected to have superior size, weight, and power requirement than a fully digital MCD and does not require a high speed A/D converter at the front end. The POC model will have a dynamic range of approximately 80 dB and will be capable of demultiplexing one thousand 64 kbps channels at 1.6 bps/Hz. Since the majority of the components are passive acousto-optic devices, this implementation of the MCD is highly reliable and radiation hard. Demodulation would be performed either serially, using a time shared demodulator, or in parallel, using an individual demodulator for each channel. One drawback to this implementation, however, is that a separate MCD is required for each separate data rate.

TRW is under contract with NASA LeRC (NAS3-25866) to develop a POC multichannel demultiplexer/demodulator (MCDD) using advanced digital technologies. The composite FDM signal is A/D converted and channelized into wideband channels of 2.048 MHz bandwidth. The wideband

channel is then either further channelized into 32 narrowband 64 kbps channels or passed directly on to the multirate demodulator as a 2.048 MHz channel. The modulation format used is differentially encoded OQPSK and the overall bandwidth efficiency of this system is 1.42 bps/Hz. The multirate demodulator can demodulate either one 2.084 MHz channel or thirty-two 64 kbps channels. This demodulator is designed as a continuous demodulator (fig. 7).

The University of Toledo is in the third year of grant (NAG3-799) to develop a programmable architecture for multicarrier demodulation based on parallel and pipeline digital design techniques for increased throughput. The hardware architecture and designs have been optimized for variable channel rates and variable numbers of channels. A POC model to demonstrate small-scale operation is under development.

LeRC has begun an in-house effort to develop and MCDD using commercial digital signal processors. The multichannel demultiplexer will be implemented as a combination of

software executing on general purpose DSP and state-of-the-art application specific DSP.

Demodulator

Once the demultiplexing function has been completed, the individual channels have to be demodulated. The present approach is to time share a bank of demodulators with each demodulator being capable of handling 24 to 32 channels.

The demodulators are presently designed to operate on continuous transmissions. which relates well to circuit switched operations. However, for packet switching, transmission is bursty. Therefore, either the demodulators will have to be capable of receiving burst transmissions or the ground terminals must transmit at regular intervals so that the continuous demodulators do not lose lock. For continuous demodulators, the ground terminals will have to send dummy packets. If the demodulators are capable of receiving burst transmissions, no dummy packets would be required. In addition, a TDM overlay could be placed on the FDMA uplinks whereby any uplink channel could be shared by multiple ground terminals.

Packet Synchronizing Buffer

The packet synchronizing buffer is

responsible for receiving data from the MCDD and assembling and aligning the packets for use by the shared decoder. Assuming that the MCDD uses a time shared demodulator, the information from the MCDD will be presented to the packet synchronizer in a bit interleaved TDM format. Each bit in the TDM frame will correspond to a particular uplink frequency channel. The packet synchronizer will buffer each user data stream to a length of $2N-1$, where N is the number of bits in a packet. The packet synchronizer will examine each user data buffer to determine the beginning of a packet and pass the individual packets -- minus the synchronizing header portion of the packet -- on to the shared decoder.

The memory requirements of this subsystem are quite large, $(2N-1)*K*L$ where K is the number of channels in each MCDD and L is the number of MCDDs in the system. If packets from individual ground terminals could be sent to the satellite so that the packets reached the satellite synchronously, the memory requirements could be reduced by approximately 50 percent. The majority of this improvement is due to the fact that an additional $(N-1)$ bits per channel is no longer required in order to be certain a full packet is captured. A second savings is achieved because there is

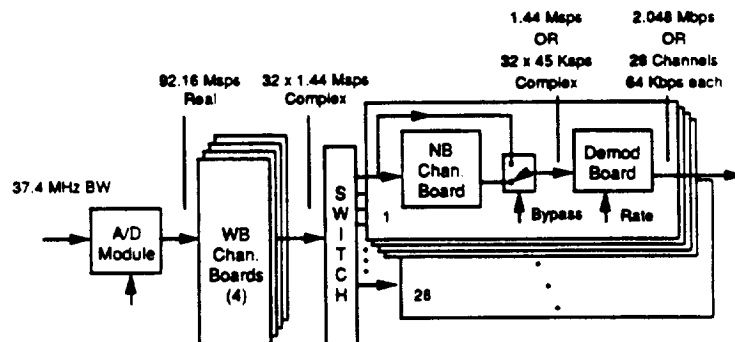


Figure 7 Digital MCDD

no longer a need for synchronization bits in the packet, thus reducing the overall packet length.

One possible method for synchronizing the uplink channels would be to the Global Positioning System (GPS). There are many commercial GPS receivers presently available. However, the cost is approximately \$500 to \$1,000 per ground terminal. By adding this additional complexity on the ground, the packet synchronizing buffer could be dramatically simplified.

Shared Decoder

The decoder subsystem decodes each packet on a packet by packet basis. Most likely, a bank of decoders will be time shared, particularly if the demodulator is time shared. Both, trellis and block decoders have been considered. If a trellis decoder were used, one could either throw away a predetermined amount of bits at the beginning of each packet in order to allow the decoder to initialize; or, one could save the previous state of the codec and jam this state into the decoder at the beginning of the next time slot for that particular source channel. For either of these methods, trellis decoding appears overly complex when consider the number or independent channels sharing the decoder. If a block decoder were used, the packet length would have to be an integer multiple of the block length. Since we have already determined that the packet will be a fixed length, the block code and packet length can readily be optimized.

Switching and Routing Elements

The switching and routing circuitry is composed of three major subsystems, the MCDD-to-Switch formatter, the 8x8 switch, and the Switch-to-TDM formatter. These three subsystem combine to effectively act

as a 8192x64 packet switch and a 256x64 circuit switch assuming 8 MCDDs with either 1024 64 kbps users or 32 2.048 Mbps users. The MCDD-to-Switch and Switch-to-TDM formatters perform the temporal routing while the 8x8 switch performs the spacial routing.

MCDD-to-Switch Formatter

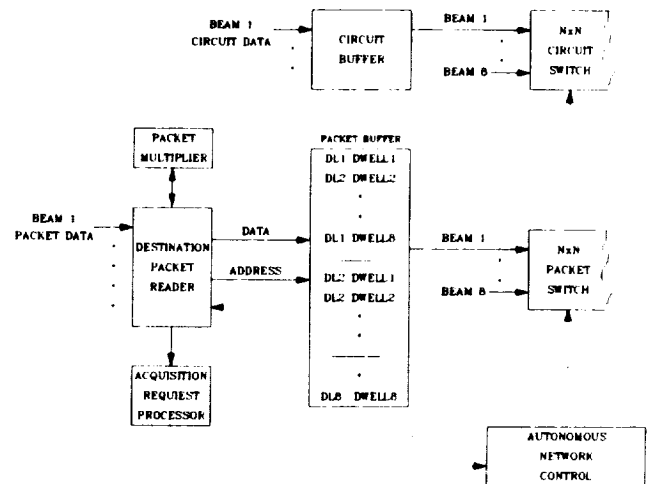


Figure 8 MCDD-to-Switch Formatter

The main function of the MCDD-to-Switch formatter is to take parallel messages and convert them into a TDM message stream (fig. 8). It receives decoded packets, examines the destination address, multiplies multicast and broadcast packets, sorts the messages, and stores the messages in a buffer for transmission through the NxN switch. In effect, the MCDD-to-Switch formatter acts as a 1024-to-64 switch with each message residing in the transmit buffer such that the messages can be transferred to the Switch-to-TDM circuitry in sequential order.

The circuitry for duplicating multicast and broadcast messages must reside in either the MCDD-to-Switch or the Switch-to-TDM formatters. Since the downlink beam address must be examined in the MCDD-to-Switch

formatter, it appears advantageous to put the packet duplication function here rather than in the Switch-to-TDM formatter. Therefore, the Switch-to-TDM formatter will only have to examine the dwell address and the downlink beam address can be discarded.

NxN Switch

The NxN switch consist of two separate switches: the 2.048 Mbps circuit switch and the 64 kbps packet switch. This portion of the overall switching system is responsible for beam-to-beam interconnects. Since this is the sole function of the NxN switch, it is possible that both the circuit and packet data utilize the same type of switching fabric -- although not necessary. Regardless, both switches must be capable of handling contention problems relative to the downlink beams. Information from two separate inputs cannot reach the same output port at the same time. This problem must either be addressed within the NxN switch or be exclude from occurring by the MCDD-to-Switch formatter.

Of the overall switching and routing system, the NxN switch may be the most straight forward portion to implement. Numerous studies and papers have been published in this area (ref. 9-15). Optical switching and neural networks have also been recently investigate to solve this type of switching problem. One promising implementation is to use a high speed time-division-multiplexed fiberoptic bus to perform the NxN switching (ref. 16).

Switch-to-TDM Formatter

The Switch-to-TDM formatter must receive data from the eight ports of the spacial circuit switch and the spacial packet switch and write that information into the proper locations of the burst transmit memory (fig 9). This must occur without loosing any

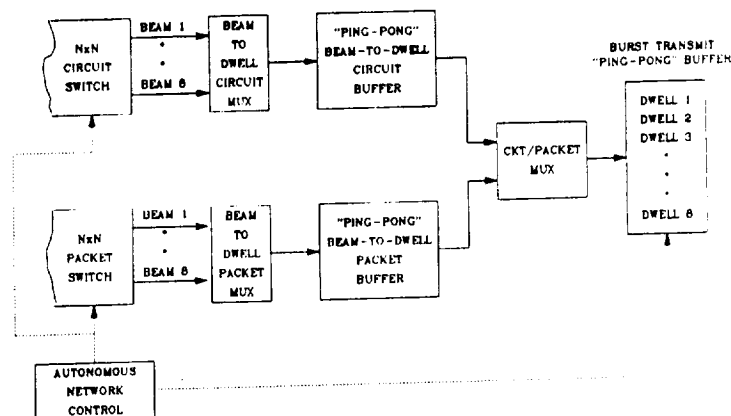


Figure 9 Switch-to-TDM Formatter

packets or circuits. Therefore, the Switch-to-TDM must be capable of resolving contention problems relative to the downlink dwell locations.

The burst transmit buffer is arranged so that each section corresponds to a particular downlink dwell location for the hopping beams. There must be reserved time slots within each dwell array for orderwires and for each 2.048 Mbps circuit destined for that particular downlink dwell. Additional memory space for each dwell is allocated by the autonomous network controller according to the "near-real-time" traffic demands of the packet network. After filling the appropriate dwell memory locations with circuit data, the Switch-to-TDM reads each packet and writes the packet to the corresponding memory location.

Encoder

The encoder is required to provide coding gain on the downlink. This encoder may be either a convolutional encoder or a block encoder capable of operating at 150 - 200 Mbps. A corresponding decoder is required at

the ground terminal. Presently, block decoders that handle these rates are available as commercial products. Convolutional decoders are much more difficult to implement. Therefore, the initial assumption is that a block encoder will be used.

Modulator

A burst modulator capable of a bandwidth efficient modulation scheme is required. A continuous phase modulation format is desired in order to run the satellite's high power amplifiers at saturation; thus, improving the downlink efficiency. NASA LeRC as an ongoing program in modulation and coding directed at such requirements. Among these are two completed contracts for 200 Mbps burst modems for satellite-to-ground applications: a 16 CPFSK modem, and an 8-PSK modem (ref. 17-18). Additional work is being performed by COMSAT Laboratories under contract NAS3-319317 for a programmable digital modem capable of binary, QPSK, 8-PSK, and 16 QAM modulation with up to 300 Mbps of data throughput.

Autonomous Network Controller (ANC)

On-board the satellite, the autonomous network controller (ANC) is responsible for allocation of the space and ground resources, and for real-time health monitoring and fault recovery of the on-board communication systems. The ANC may not perform all of the required network control functions; however, a favorable distribution of the network control functions will be realized between the on-board ANC and a ground-based network controller. In particular, traffic allocation and routing functions will be placed on-board to shorten call set-up and disconnect times. The ANC responds to narrowband user connection requests by allocating an uplink frequency to the requesting terminal.

The ANC will also allocate downlink time slots for 2.048 Mbps circuit switched data. The ANC will monitor the downlink burst buffers capacity, forward the burst buffer status to the ground terminals via downlink orderwires, and vary the length of the downlink dwells to accommodate changing traffic patterns. In addition, the ANC will control the burst transmissions and the hopping beam antenna system.

CONCLUDING REMARKS

From an overall systems view, the problem of getting tens of thousands of low data rate users to communicate with each other through a processing satellite is of equal complexity whether it is accomplished using TDMA/TDM, FDMA/TDM, CDMA/TDM or another type of architecture. FDMA and more recently CDMA techniques have been touted as being superior to TDMA because of the reduced uplink transmit power required versus TDMA which, in turn, implies reduce ground terminal cost. These techniques, however, mandate that extremely complicated functions be performed onboard. In fact, all the functions from the MCDD to the transmit buffer of the MCDD-to-Switch formatter are necessary to get to a point that looks very similar to a TDMA uplink.

Any onboard processing system requires fault tolerant implementation. With size, weight, and power at a premium, traditional fault tolerant methods such as simple two-for-one redundancy of components and systems or majority voting will not suffice. NASA LeRC plans to address these issues in all aspects of the ISP design and is pursuing innovative fault-tolerant approaches which optimize redundancy requirements. Presently, the issue of fault tolerance in the digital multichannel demultiplexer is being addressed through a grant with the University of California, Davis

(NAG3-1166).

The present data rates of 64 kbps and 2.048 Mbps were chosen as a starting point and to be compatible with terrestrial ISDN networks. It is understood that these data rates may not be optimum. In particular, the uplink transmission rates will most certainly be slightly higher in order to accommodate the increase overhead inherent in a packet switched network.

STATUS AND FUTURE DIRECTIONS

NASA plans to develop a proof-of-concept (POC) information switching processor. The POC model will be constructed in-house at the NASA Lewis Research Center. In-house developed POC hardware will be supplemented by advanced fault tolerant components developed under contracts. The ISP architecture will ultimately be demonstrated in an satellite network simulation by integrating the ISP with high speed codecs, programmable digital modems, and multichannel demultiplexer demodulator currently being developed under industry contracts and university grants (ref. 19), and compatible ground terminals and on-board and ground based network control.

ACKNOWLEDGEMENTS

The authors wish to acknowledge the ISP Architecture Study Team members: Mr. James Budinger, Mr. Eric Bobinsky, Mr. Grady Stevens, Mr. Jorge Quintana, Mr. Nitin Soni, Mr. Heechul Kim, Mr. Paul Wagner, Mr. Mark Vanderaar and Dr. Pong Chu for their important contributions to the satellite network architecture and the ISP architecture.

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